An Improved Resonant Gate Driver for MOSFETs in DC-DC Converters

Hamza Yapici[1] and Remzi İnan[2]

[1] Department of Electronics and Automation, Necmettin Erbakan University, 42310 Konya, Turkey, hyapici@erbakan.edu.tr

[2] Department of Electric and Electronic Engineering, Isparta University of Applied Sciences, 32260 Isparta, Turkey, remziinan@isparta.edu.tr

Abstract: The Resonant Gate Drivers (RGDs) have a key role in increasing switching performance, facilitating the integration of gate drivers with converters and reducing the gate loss of discrete components, such as power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Silicon Carbide (SiC) MOSFETs and insulated gate bipolar transistors (IGBTs) at high switching frequencies to promote the integration level of gate drivers with power modules. In this paper, an improved non-complex, and low-cost RGD, with an air core inductor and an adjustable duty ratio in high switching frequencies is proposed for discrete MOSFETs. The RGD that may provide less leakage current proposed in this paper uses MOSFETs, bipolar junction transistors (BJTs), and a few passive components. In addition, another focus is to eliminate the oscillations between gate-source terminals that force the limits of breakdown voltage between drain-source terminals and cause excessive thermal losses and failures on discrete components. The gate driver also includes four stages; the small signal-switching circuit, the signal amplitude-shifting circuit, the B-type push-pull circuit containing transistors connected by the totem pole technique and resonant circuit based on air core inductor. The last stages ensures the controlling of charge-discharge of the input capacitance of the MOSFET and reduces power consumption, thus, the peak voltages during the turn-on stages are also decreased. The power MOSFET with high input capacitance in a DC-DC converter is used to verify the experimental vaidation. In addition, the results of the experimental study, based on switching frequancy and total power consumption, are compared with some other RGDs introduced in the literature.

Keywords: B-type push-pull circuit; BJT-based driver; power MOSFETs; pulse width modulation; resonant gate driver

1 Introduction

Today, the interest in environmentally friendly Renewable Energy Sources (RESs) is increasing, due to the decrease in fossil fuels and the increasing environmental problems, caused by the effects of fossil fuels [1]. As a result, the components of

RES-based systems such as battery energy storage systems (BESSs), high-frequency driver circuits, and power generation devices are also being improved by researchers' day by day. Recently, solar energy [2] and power electronics [3] based systems have also attracted much attention. The gate drivers are a promising circuit used to save power loss at high switching frequencies [4]. One considerable application is high-frequency gate drivers, for generating input signals to drive boost converters integrated into stand-alone or grid-connected systems [5].

Despite requiring high DC voltage that supplies the DC loads and input of the inverters, especially in low power applications DC RESs, usually generate a voltage of less than 50 V. In high-voltage inverter applications which include photovoltaics (PVs) and BESSs, step-up converters are used to increase the produced voltage level to 380 V − 400 V [6]. Turning on MOSFETs becomes more complex as the voltage increases [7]. Nevertheless, the gate-drivers, with switching frequencies currently reaching 1 MHZ, have been proposed to reduce switching losses and improve converter performance [8]. These drivers are used not only for MOSFETs but also for IGBT and other semiconductor components [9]. In recent years, the SiC and power components have been widely used in high-voltage applications due to their high switching capability [10]. On the other hand, the design, and the performance evaluation of the high-power MOSFET drivers have been the subject of many studies such as transient immunity [11], modular multilevel converter [12], PV inverter applications [13], high current applications [14], medium-voltage application [15], parallel operation converters [16], high power applications, overcurrent protection applications [17], junction temperature estimation of gate-driver [18].

The drivers of Silicon-based, SiC and Gallium-Nitride-based MOSFETs can be examined into three main categories. These categories include isolated drivers using optical integrated circuits (ICs) and AC coupling techniques, and non-isolated drivers designed using resonant circuits and some components [7]. Early studies focused on gate driver circuits, which contain resonant drivers with a small number of components in MOSFET applications [19]. Thus, gate driver performance is related to the energy of the equivalent circuit capacitors [20]. In resonant drivers, using an inductor affects the turn-on and turn-off speed performance of MOSFETs [21]. Such drivers have been developed and implemented for high-speed applications. These converters are not only less complex but also efficient and well-regulated [22]. Furthermore, in no-loads conditions, high losses occur and there may be distortions in the output regulation [23]. On the other hand, drives with isolation transformers are also designed, which greatly reduces the on-off time [24]. Moreover, high-side gate drivers are designed using a current-mode differential error amplifier [25]. For high-side and low-side drivers, the current sensing IR21XX series ICs are produced which are used at different voltage and current levels [26] Also IR2125 series ICs are used to limit the loop current and operate the bootstrap [27]. In addition, snubber [7], bootstrap [28], and charge-pump circuits [29] are used for MOSFET gate drivers. However, these circuits are not adaptive and have current

and voltage limits. They are also difficult to use in a wide duty-cycle and power ranges.

MOSFETs used in buck and boost converters are under high power stress due to the voltage induced on the switching element and the load current flowing through it, and this creates difficulties in turning off MOSFETs [30]. For this reason, hard-switching techniques should be used in switching MOSFETs. However, at high frequencies, switching losses increase and efficiency decreases. High power density converters have been developed in power electronics applications by increasing the switching frequency with soft switching methods such as zero-voltage switching (ZVS) and active clamp [31]. The ZVS and zero current switching (ZCS) [32] approaches can be preferred to reduce losses in high frequencies. Although these methods reduce the losses in practical applications, it is not possible to be zero the switching power losses [33]. The ZVS-based inverters with a ground-ended transistor have advantages at high frequencies. However, the harmful peak voltage on drain-source voltage may occur [34]. The main problem of the active clamp method is performance degradation at light loads due to the snubber capacitor discharging time interval. Also, large leakage inductances are required for operation over a wide range of power. This causes unwanted duty cycles, extra losses and voltage drop. On the other hand, the drives designed with the ZVS method are complex and increase the cost of devices. [31].

The voltage level and the operating frequency determine the main criteria for selecting the topology of MOSFET gate drivers [35]. In Gate driver applications for MOSFETs introduced in [36], and [37], Schottky diode circuits, bipolar totem-pole driver circuits, turn-off diode methods, PNP/NPN turn-off circuits and IR series ICs are frequently used. In [38], a gate-driver capable of operating at high temperatures has been designed for electric vehicle motors. In addition, two basic protection functions are adopted for the driver. The first of these functions is desaturation detection and the second one is crosstalk suppression. An isolated gate driver has been proposed in [39], to limit the leakage current of discrete components such as MOSFETs and BJTs. The designed driver provides isolation and amplification. For isolating the signal, a CMOS-based isolation circuit has been preferred. The authors used the BJT-based push-pull driver and the voltage level shifter circuit to amplify the signal. In [40], the authors proposed an opto-isolator-based gate driver for motor control applications. The proposed driver with low breakdown probability has been used for medium frequency levels. The authors presented a gate driver in [41], including the switched capacitor for multilevel converters. The proposed model eliminates common mode noise, reduces common mode capacitance, and improves transient immunity. In [42], the authors proposed a ZCS method for bidirectional DC-DC converters for electric vehicles and aimed for attaining the zero current turn-off operation of the switching components.

In addition to the difficulties described for the driver circuits mentioned above, conventional drivers have high switching losses and are difficult to control at high frequencies. This situation can be overcome using resonance driver techniques [43].

However, the variation of voltage and current limits the response of conventional resonant circuits. Driver circuits designed using auxiliary MOSFETs [44] are not cost effective, and an additional driver circuit is required. Also, for ICs, the negative voltage of the source pin of ICs (V_s) defined for the voltage supply of the ICs is one of the biggest problems of bootstrap circuits. This situation is caused due to the disadvantage that occurs from the load current circulating through the resistor [7]. In this study, a new simple and cost-effective RGD, which contains four layers, is proposed to drive the power MOSFETs used in DC-DC converters designed for grid-connected PV-home systems. The discrete transistors can operate at high power applications, and they are resistant to current-voltage changes of the load [45], thus, the driver circuit is not affected by load changes, high currents and voltage fluctuations which are appeared due to the load changes. The main concept is to handle the resonant inductor and the totem-pole structure [34] for driving MOSFETs. The voltage and the current generated by the microcontrollers are not sufficient to drive SiC and power MOSFETs [38].

In this study, it is aimed to improve the approach which is given in [38] by amplifying the voltage level of the output signals of the pulse generators or microcontrollers. For this purpose, an air core inductor-based approach is applied to design a gate driver. In the first part of the driver, the MOSFET-based circuit, where the PWM signal is applied, is used to reduce the time delay between input and output, and then to ensure stable operation of the driver. In the second part, the voltage level shifting circuit as given in [39] is adopted to boost the pulse width modulation (PWM) signal to 12 V. In the third part, the B-type push-pull circuit containing the NPN and PNP base transistors is used to turn on and off the MOSFET. A low value external gate resistance (R_G) is connected to both transistors to reduce the losses that occur during the turn-on stage. In the last part, an air core resonant inductor (L_F) is connected in series to R_G for reaching high frequencies, suppressing transient oscillations, and reducing losses.

The main contributions of this study are:

1) By using an air core inductor, switching at high frequencies is guaranteed, and the power consumption of the MOSFET is reduced by charging and discharging the input capacitance in a low time delay.

2) In the resonance part, the resonant inductor (L_F) is connected in series to R_G. Moreover, to prove the stability and capability of the proposed circuit, it is compared with a few drivers proposed in the literature and the gate driver designed with IR2121 integrated circuit.

3) To design the simple and cost-effective MOSFET driver circuit with high control performance and stable operating characteristics, by using integrated circuit technologies whose supply process is not difficult.

4) To prevent the negativities in the supply of switching driver integrated circuits due to the shortage of semiconductor material production today.

For this purpose, a real-time MOSFET gate-driver circuit with the following features is designed by using the switching techniques available in the literature and adapting the methods to PV-based converter applications by modifying the methods.

5) Using the least number of components to reduce the complexity and the costs of the driver.
6) Due to the power BJT characteristic, for MOSFETs, the ability to operate in transient conditions such as overvoltage, and voltage sag.
7) Reading the power consumption and voltage levels using feedback components for various duty-cycle ratios. Thus, the proposed RGD will be able to generate the variable PWM signal.
8) The capability to generate PWM signal at $0 - 1$ MHz and up to 90% duty cycle.

In this study, the proposed RGD is compared with some gate drivers in terms of power consumption, cost, and switching frequency. The proposed driver achieved at least, equal results of the drivers in the current literature.

In this study, Section 2 describes drive design and operation, Section 3 includes experimental analysis, Section 4 concludes the paper, discussing advantages and disadvantages.

2 Design and Operation Principle of the Proposed MOSFET Gate Driver

2.1 The Main Design

Generating high-frequency PWM signals for DC-DC converters in grid-connected PV systems with BJTs instead of MOSFETs may reduce passive components and provide cost savings. In addition, as mentioned before, these BJTs can operate at high current and voltage values and are less affected by load changes due to their characteristics.

The BJT-based non-inverting totem-pole drivers are the most popular and cost-effective circuits for driving MOSFETs. As external drives, these circuits improve the operating conditions of the PWM controller by optimally controlling current gains and power losses. The driver circuit must be placed close to the location of power MOSFETs on the circuit. Thus, when driving the MOSFET gate terminal, high current transients are localized in a minimal loop area and the value of parasitic inductances is reduced [46]. R_G is optional in the circuit and can be selected to provide the required gate impedance depending on the DC gain (β) of the

transistors. In these circuits, the transistors protect each other against failure. Assuming the R_G is negligible, this can clamp the gate voltage V_G as $-V_{BE} < V_G < V_{bias} + V_{BE}$ interval, where V_{BE} is the base-emitter voltage of BJTs and V_{bias} is the bias voltage, V_G is the external gate voltage. Moreover, NPN-PNP totem-pole drivers do not require Schottky diodes [37].

The turn-on and the turn-off states can be examined in four basic time periods. In the first sate, the gate driver charges the gate source capacitance (C_{gs}) and gate drain capacitance (C_{gd}) via R_G during the first period. In the end of the time interval, the gate source voltage (V_{GS}) equals the threshold voltage (V_{TH}) of MOSFETs. In the second period, the further increase in V_{GS} voltage ensures the flowing of the drain current (I_D). During the third period V_{GS} is constant, and this is known as the Miller effect (see more details for the Miller effect in [37]). In the last period, the gate of the MOSFET reaches oversaturation. C_{gs} is charged till V_{GS} is equalized to the supply voltage. In this time interval, the MOSFET has no switching losses. In the turn-off state, V_{GS} starts to decrease in the first period. Thus, with the onset of exponential reduction of I_G, C_{gs} and C_{gd} begin to discharge. In the second time interval, the drain source voltage (V_{DS}) increases to the last value of the drain source voltage of turn-off stage ($V_{DS(off)}$), from $I_D \times R_{D(on)}$, where $R_{D(on)}$ is the on-resistance of MOSFETs. During this period, V_{GS} is constant and at the end of the period, V_{DS} equals the DC bus voltage. So, the Miller effect occurs for the turn-off state during this interval. In the third time interval, the I_D decreases towards the value in the turn-off-state conditions. In this event V_{GS} is still constant. In the fourth time interval, V_{GS} decreases towards values below V_{TH}. The Gate current charges the power state capacitance between drain and source (C_{ds}) and simultaneously C_{gs} discharges. At the end of the period, the MOSFET is completely switched off [7].

In this study, the step-up converter containing IRFP460 type MOSFET which different manufacturers can supply is preferred for testing the proposed driver circuit. The parameters of this MOSFET are available in [47]. During turn-on and turn-off, the change in V_{DS} is controlled by I_G. The required I_G is given in Eq. 1. Also, the simple model of MOSFETs presented in [34] is given in Figure 1.

$$I_G = \frac{dQ}{dt} \tag{1}$$

At the turn-on stage, I_G can be expressed as $(V_G - V_{TH})/(R_o + R_G)$. Also, at the turn-off stage, I_G can be expressed as $(V_G - V_D)/(R_o + R_G)$. If a fast-recovery diode is used, then it can be expressed as $(V_G - V_D)/(R_o + R_{diode})$. Where Q is the charge accumulated between gate and source of MOSFETs, V_G is the external gate terminal voltage, R_o is the output impedance of MOSFETs, V_D is the external drain terminal voltage and R_{diode} is the internal resistance of diode of power MOSFETs. On the other hand, the amplitude of the drive output must be set to the appropriate level without ignoring the catalog values, due to the I_D depends on the V_{GS} value as shown in Eq. 2.

$$I_D = I_{DSS} \cdot \left(1 - \frac{V_{GS}}{V_{TH}}\right)^2 \quad (2)$$

where I_{DSS} is the zero-gate voltage drain current.

The resonant inductor at switching frequency can be calculated as in Eq. 3. L_F, resonating with the C_{iss}, is obtained as 471 nH, where the turn-on speed [34] is 3% of the switching period. Similar to the method discussed in [39], a push-pull circuit is adopted. Differently, the high-speed NPN and PNP-based single-layer structure is considered to reduce delays. Also, isolation transformer is not used for this application due to variable current and voltage values constraints. Instead of a high-frequency transformer, a layer provided self-isolation designed with MOSFET. This layer not only ensures that the current of the microcontroller is more stable, but also decreases the time delay of the driver at high frequencies. As seen in the Eq. 4, the output current of the BJTs depends on the β value [48]. Note that, C_{iss} is the input capacitance of MOSFETs, C_{oss} is the output capacitance of MOSFETs, C_{rss} is the reverse transfer capacitance of MOSFETs.

$$L_F \leq \frac{4}{C_{iss}} \left(\frac{\text{turn on speed of MOSFET}}{\pi \,.\, \max(f_{sw})}\right)^2 \quad (3)$$

The driver circuit is shown in Figure 2. The DC source voltage V_{CC} and GND are the positive and ground rails used by all layers, respectively.

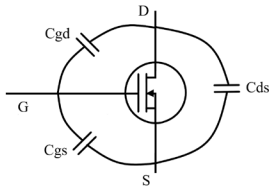


Figure 1

$$I_{B,min} = \frac{I_{C,max}}{\beta_{max}} \quad (4)$$

Where, $I_{B,min}$ is the minimum base current, $I_{C,max}$ is the maximum collector current and β_{max}, which is given in manufacturers datasheet, is the maximum DC gain of BJTs. On the other hand, the total gain of the push-pull circuit depends on the total gain of the whole connected circuits [39]. The high-gain transistor in the second layer compensates for the switching losses at high frequencies. It provides the current amplification necessitated, allowing a single layer structure [7] instead of using a multi-level push-pull drive circuit and reduces the time delay caused by transistors. One of the protection ways for MOSFETs against immediate differential voltage deviation (dv/dt) occurring during switching is to connect a resistance between the gate and source [36]. As shown in Figure 2, the first layer is connected

through this pull-down resistance ($R_{G,1}$) to the PWM generator and its value is bounded and determined as follows:

$$R_{G,1} \leq R_S + R_G + R_{G,int} \tag{5}$$

where, $R_G = \left(V_{in,pwm} - V_{TH}\right)\left(t_{on}/Q_{gd}\right) - R_S$, $Q_{gd} = V_G\left(C_{gd} + C_{gs}\right)$, R_S is the internal resistance of PWM source, $R_{G,int}$ is the internal resistance of MOSFETs, $V_{in,pwm}$ is the maximum amplitude of PWM signal, V_G is the gate terminal voltage, t_{on} is the on-state time, Q_{gd} is the gate-source charge and $C_{gd} = C_{rss}$ and $C_{gs} = C_{iss} - C_{rss}$. Due to the power supply provides less current, $\ll 1A$, R_G is not used. Thus, it can be assumed that $V_G = V_{in,pwm}$. Moreover, the damping resistor $R_{D,1}$ is:

$$R_{D,1} = \frac{V_{CC} - V_{DS}}{I_D} \tag{6}$$

where, V_{CC} is the source voltage. The maximum value of $R_{D,1}$ is calculated when $V_{DS} = 0V$. $R_{D,1}$ is calculated as $34.48\ \Omega$, however, due to the thermal conditions of the real-world applications, $R_{D,1}$ is selected as $300\ \Omega$.

The total power loss of a MOSFET is the sum of the switching losses and conduction losses. The conduction losses only occur on resistances [34]. The switching losses occur within the time periods that include moment when I_D rises from 0 A to $I_{D,max}$ value and V_{DS} falls from its maximum value to 0 V or vice versa [37]. The total power losses can be expressed as:

$$P_{loss} = P_{RD} + P_{CON} + P_{SW} \tag{7}$$

P_{RD} is the thermal loss occurred on R_D and is expressed as $(I_D)^2 R_{D,1}$. P_{CON} is the conduction loss and P_{SW} is the switching loss. Assuming the resistive impedance for MOSFETs, P_{CON} and P_{SW} can be expressed as below:

$$P_{CON} = I_D^2 R_{D(on)} \frac{V_{DS}}{V_G} \tag{8}$$

$$P_{SW} = \frac{V_{DS} I_D}{2}(t' + t'')f_{sw} \tag{9}$$

where, $V_{DS} = V_{CC} - I_D R_{D,1}$, t' is the time interval that includes when I_D rises from 0A to $I_{D,max}$ and t'' is the time interval includes that when V_{DS} falls from its maximum value to 0 V. From [36], the time intervals is express as follows: $t' = C_{iss}\left(V_{GS,Miller} - V_{TH}\right)/I'_G$ and $t'' = C_{rss}/I''_G$, where $V_{GS,Miller}$ is the voltage amplitude at Miller effect, $I'_G = \left(V_{in,pwm} + 0.5\left(V_{GS,Miller} - V_{TH}\right)\right)/(R_{S,H} + R_G + R_{G,int})$ and $I''_G = \left(V_{in,pwm} - V_{GS,Miller}\right)/(R_{S,L} + R_G + R_{G,int})$. Note that, it is assumed that $R_{S,L} = R_{S,H}$ for PWM generator based on $R_{G,int} \ll R_S$ and $R_G = 0$.

The power consumption (P_G) for charging the gate capacitance depends on the switching frequency (f_{sw}) and the energy transferred to the gate terminal (E_{tr}), and is calculated as follows:

$$P_G = E_{tr}.f_{sw} = \left(C_{gd} + C_{gs}\right).V_G^2.f_{sw} \quad (10)$$

It is important that V_G cannot be increased too much to reduce power consumption. Also, the power consumption P_C for charging output capacitance is given below:

$$P_C = \frac{1}{2} C_{oss} V_G^2 f_{sw} \quad (11)$$

Si-based BJTs for low-power applications have been used since the 1980s. For fast switching at low power, the BJTs are kept saturated during on-state and the base-emitter capacitance C_{be} must be charged and discharged rapidly [48]. For a low-power application, a simple structure is sufficient.

During the turn off interval of the MOSFET located on the first layer, the BJT used on the second layer, named Q_2, is turned on. During this period, the power losses occur on base-emitter junction and base-emitter capacitance. Also, at this interval, the power loss P_{RC} occurs on R_C as thermal loss and is proportional to I_C^2. The value of the R_C resistor can be calculated with the equation of $R_C = V_{CC}/I_{C,saturation}$, where $I_{C,saturation}$ is the collector saturation current. Thus, $R_{C,2}$ is calculated as $120\ \Omega$. The power loss of base-emitter junction P_{B-E} is obtained as follows:

$$P_{B-E} = I_B V_{BE,sat} \quad (12)$$

where, I_B is the base current, $V_{BE,sat}$ is the base-emitter saturation voltage. I_B can be calculated as:

$$I_B = \left(\frac{I_{sat}}{\beta}\right) e^{-\frac{V_{BE}}{v_T}} \quad (13)$$

where, I_{sat} is the saturation current, v_T is the thermal voltage which equals to $kT/q = 26$ mV, k is the Boltzmann coefficient, T is the temperature given as °K, q is the electronic charge. The term of $I_{sat}e^{-V_{BE}/v_T}$ which exists in the expression of I_B is equal to the collector saturation current $I_{C,saturation}$.

The power consumed for charging C_{be} is expressed below:

$$P_{C_{be}} = f_{sw} Q_B V_{BE} \quad (14)$$

where, Q_B is the minority-carrier charge and equals to $\Delta V_{BE} C_{be}$. Note that $\Delta V_{BE} < 26$mV at 25℃ in general assumptions. In real-time applications, ΔV_{BE} is taken as ~ 10mV. Also, the power consumption on R_B is calculated as:

$$P_{R_B} = I_B^2 R_B \quad (15)$$

where, $R_B \leq (V_{CC} - V_{BE})/I_{B,min} - R_D$, and $I_{B,min} = I_{C,saturation}/\beta$. Thus, $R_{B,2}$, which is the external base resistance of Q_2, is calculated and taken as $0.75\ \Omega$.

As shown in Figure 2, the NPN transistor in the third layer identified as Q_3 is supplied by the common DC source. On the other side, the collector terminal of the PNP transistor which is labeled as Q_4 is directly connected to the ground. During

the turn-off period of the second layer, the Q_3 is ON and this time interval is called as on cycle. In contrast, during the turn-on period of the second layer, the Q_4 is ON and this time interval is called as called off cycle. During the on cycle, the dc current $I_{C,DC}$ flows through the resonant layer along the power MOSFET. On the other hand, during the off cycle, the input capacitance discharges with $I'_{C,DC}$ through the Q_4. $I_{C,DC}$ and $I'_{C,DC}$ are calculated as follows:

$$I_{C,DC} = \frac{V_{CC} - V'_{GS}}{R_G + R_{G,int}} \tag{16}$$

$$I'_{C,DC} = \frac{-V'_{GS}}{R_G + R_{G,int}} \tag{17}$$

$$R_G = 2\sqrt{L_F / C_{iss}} - R_{TP} - R_{G,int} \tag{18}$$

where, R_G is the external resistance connected to the power MOSFET and is calculated with (18), R_{TP} is the output resistance of the push-pull circuit and $R_{G,int}$ is the internal resistance of power MOSFET, V'_{GS} is the internal gate-source voltage and equals to $Q_{gd}/(C_{gd} + C_{gs})$. In general, the DC gain that determines the collector current of BJTs varies within a certain range. To reduce the effects of this manner, $R_{B,3}$ can be selected as $R_{B,3} \ll (1 + \beta_4)R_G$ [9], since β_3 is larger than β_4, $R_{B,3}$ is handled as 0.91Ω by considering β_4. β_3 is the dc gain of the Q_3, β_4 is the dc gain of the Q_4, and $R_{B,3}$ is the external base resistance of push-pull circuit.

In (18), $R_{G,int}$ is given as 1.8Ω as mentioned in [47]. Here, R_{TP} can be handled as $1/h_{oe}$. h_{oe} is the output admittance and obtained from datasheets. Also, $1/h_{oe}$ can be taken into account as an open circuit. Thus, the expression in (18) can be rearrange as $R_G = 2\sqrt{L_F/C_{iss}} - R_{G,int}$, and R_G is obtained as $\sim 11\ \Omega$. However, for higher input capacitance of MOSFET, R_G is considered as $3.3\ \Omega$.

Assuming that the Miller effect is negligible for BJTs used in proposed design, the switching losses occuring on Q_3 and Q_4 are given in (19) and (20), respectively.

$$P_{Q_3} = f_{sw}(R_G + R_{G,int})C_{iss}V'_{CE,sat}I_{C,DC} \tag{19}$$

$$P_{Q_4} = f_{sw}(R_G + R_{G,int})C_{iss}V''_{CE,sat}(-I'_{C,DC}) \tag{20}$$

where, $V'_{CE,sat}$ is the collector−emitter saturation voltage of Q_3 and $V''_{CE,sat}$ the collector−emitter saturation voltage of Q_4. Since the input impedances h_{ie} and output admittances h_{oe} of NPN and PNP transistors are accepted as less than 1 ($h_{ie} \ll 1$ and $h_{oe} \ll 1$), thus the conduction power loss of BJTs will be neglected. By neglecting the inductor core loss, the consuming power of the resonant stage of the RGD (P_{Res}) is given as:

$$P_{Res} = (I_{C,DC})^2 R_G \tag{21}$$

Note that the parasitic parameters [45] may cause unwanted voltage fluctuations on MOSFET. However, this issue will not be addressed in this study. The power losses calculated above are listed in Table 1. The MOSFET used in the first layer is BS170 which is N channel transistor. The BJT handled in the level shift layer is BC548 which is applicable for high-speed switching applications. The BJTs used in the push–pull circuit are BC556a and 2N222a which are PNP and NPN type transistors, respectively. The parameters of these transistors are given in [49-51] and [52], respectively. Since the BS170 does not fully turn on at the high level of the input voltage, it turns off easily at the low level of the input. Thus, no additional components are required.

Table 1
The power losses obtained

Power Loss (μW)	P_{RD}	P_{CON}	P_{SW}	P_G	P_C	$P_{C_{be}}$	P_{B-E}
	272.75	2.616	4.004	600	212.5	0.049	2.284×10^{-7}
Power Loss (mW)	P_{Q_3}	P_{Q_4}	P_{Res}	P_{R_B}			
	9.99	9.98	148	12			

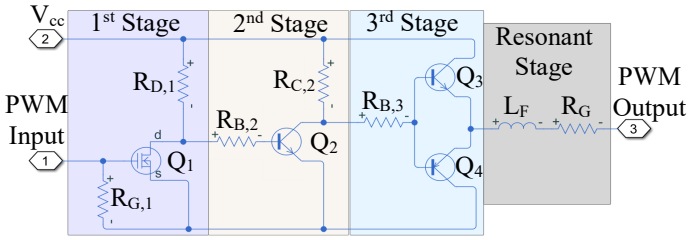


Figure 2
The proposed circuit of gate drive circuit

2.2 The Operational Principles

In the interval of on-cycle, Q1 is ON, Q2 is OFF and Q3 which allows the C_{iss} to be charged is ON. The I_L is raised by V_{CC}, therefore, V_{GS} ramps up and the MOSFET in the converter switches on. At the end of this period, C_{iss} is fully charged. The turn-on time t_{on} can be calculated as follows:

$$t_{on} = t_1 + t_2' + t_3 \tag{22}$$

where, t_1 is the turn on time of BS170, t_2' is the turn off time of BC548, and t_3 is the turn on time of 2N2222a. In this interval, at the rise time named Resonant Stage, the gate current I_G which is expressed as a second-order equation and the gate-source voltage V_{GS} can be calculated as follows:

$$I_G = \frac{V_{CC}}{L_F}\left(\frac{1}{(s+\alpha)^2 + w_d^2}\right) \tag{23}$$

$$V_{GS} = V_{CC}\left(1 - \frac{\alpha}{w_d} e^{-\alpha t} \sin w_d t - e^{-\alpha t} \cos w_d t\right) \quad (24)$$

where, $\alpha = \frac{R_G + R_{g,int}}{2L_F}$, $w_d = \sqrt{w_0^2 - \alpha^2}$, $w_0 = \sqrt{\frac{1}{L_F C_{iss}}}$

The internal gate resistance $R_{g,int}$, which is the is a damping element, is lower than characteristic impedance Z_0. Z_0 is equal to $\sqrt{L_F/C_{iss}}$. At the end of the rise time, V_{GS} equals the source voltage V_{CC}. Where, α is the damping coefficient, w_d is the ringing frequency, and w_0 is the resonant frequency. At the clamping time, the MOSFET is fully charged and the current flow through the inductor is 0, so, I_G is 0. Hence, V_{GS} remains constant during this time.

In the interval of off cycle, Q1 is OFF, Q2 is ON and Q3 is OFF, where the C_{iss} is discharged through the L_F, R_G and Q4. In other words, At the beginning of this interval, named the damping stage, C_{iss} starts to discharge and V_{GS} starts to decrease to 0. The turn-off time t_{off} can be expressed as given in Eq. (25). At the end of damping stage, V_{GS} is 0. I_G and V_{GS} can be calculated as follows:

$$t_{off} = t_1' + t_2 + t_3' \quad (25)$$

$$I_G = \frac{-V_{CC}}{L_F w_d} e^{-\alpha t} \sin w_d t \quad (26)$$

$$V_{GS} = -V_{CC}\left(-\frac{\alpha}{w_d} e^{-\alpha t} \sin w_d t - e^{-\alpha t} \cos w_d t\right) \quad (27)$$

where, t_1' is the turn off time of BS170, t_2 is the turn on time of BC548, and t_3' is the turn off time of 2N2222a. Considering the turn-on and turn-off times, it is estimated that the proposed RGD will operate at a frequency of 1 MHz. The flowchart of the design procedure and analysis for the proposed driver is depicted in Figure 3.

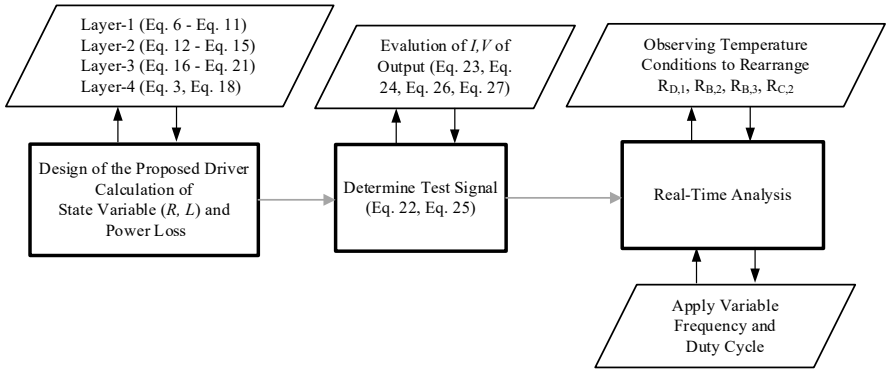


Figure 3
The flowchart of the desing procedure

3 Experimental Analysis of The Proposed Gate Driver

In this section, performance analysis is carried out by testing the gate driver circuit detailed in the previous section. To prove the performance and the stability, the proposed driver is compared with a few drivers introduced in literature and with IR2121 MOSFET gate-driver produced by International Rectifiers Corporation. The proposed driver circuit is analyzed in the following two main parts: (1) No-load test, (2) test under load (testing by connecting to the boost converter). Figure 4 demonstrates the test setup. Also, Figures 5a and 5b show the views of the upper side of the PCB of the proposed gate driver and the circuit of IR2121 integrated circuit which is used for comparison.

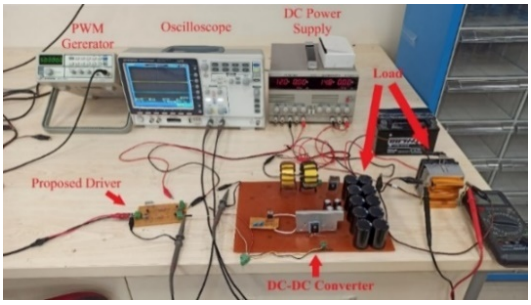
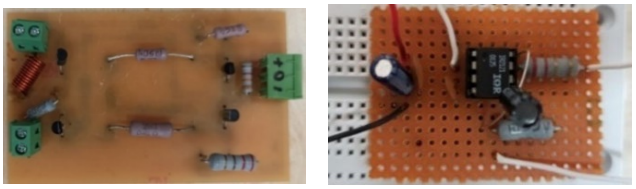


Figure 4
The experimental study setup



(a) (b)

Figure 5
The views of the upper side of the PCB of the gate drivers designed for the power MOSFETs: a) the proposed gate driver, b) the gate driver designed with IR2121 integrated circuit

The parameters of the proposed design in all analyses performed are presented in Section 2, and the results of real-time tests are presented in Subsection 3.1 and Subsection 3.2. The findings obtained as a result of the analyses are given in Table 2, Table 4, and Table 5. The losses given in the tables in subsections below match the losses obtained by equations given in previous section. Switching frequency is chosen as a criterion according to Eq 3. Rise/fall time depends on the electrical characteristics of the selected switching elements. The electrical characteristics of MOSFET and transistors are listed in Table 2 and Table 3, respectively.

Table 2
The parameters of BS170

Parameter	Limit
Drain-Source Voltage (V_{DS})	60V
Gate-Source Voltage (V_{GS})	$\pm$20V
Drain Current – Pulsed (ID)	0.5A
Operating Junction and Storage Temperature Range	-55 to 150 °C
dV/dt	–
C_{iss} @1MHz, $V_{DS} = 10V$	40pF
C_{oss} @1MHz, $V_{DS} = 10V$	30pF
C_{rss} @1MHz, $V_{DS} = 10V$	10pF
Total Gate Charge (Q_g)	–
Turn-On Time @$V_{GS} = 10V$, $I_D = 0.2A$, $V_{DD} = 25V$, $R_g = 25\Omega$	10ns
Turn-Off Time @$V_{GS} = 10V$, $I_D = 0.2A$, $V_{DD} = 25V$, $R_g = 25\Omega$	10ns
Gate Input Resistance ($R_{g,internal}$)	–
Reverse Recovery Time of Body Diode	–

Table 3
The parameters of BJT transistors

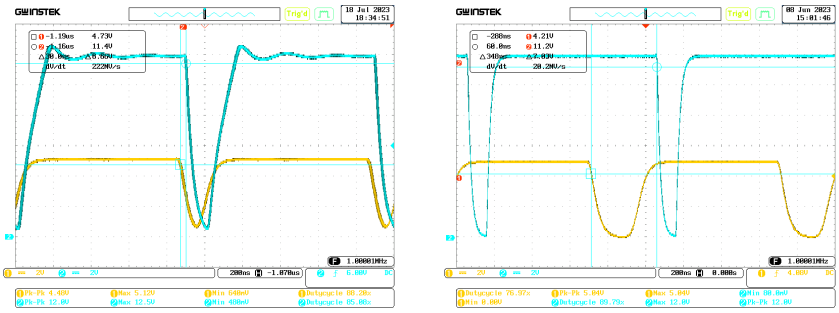
Parameters	BC548c	BC556a	2N2222a
Collector-base voltage (V_{CBO})	30V	−80V	75V
Collector-emitter voltage (V_{CEO})	30V	−65V	40V
Emitter-base voltage (V_{EBO})	5V	−5V	6V
Dc collector current (I_C)	100mA	−100mA	600mA
Dc current gain (h_{fe})	110 − 800	110 − 800	35 − 100
Collector emitter saturation voltage ($V_{CE(sat)}$)	200mV	−300mV	300mV
Base emitter saturation voltage ($V_{BE(sat)}$)	900mV	−900mV	1200mV
Base emitter on voltage ($V_{BE(on)}$)	660mV	−660mV	–
Current Gain Bandwidth (I_C)	300MHz	150MHz	300MHz
Output Capacitance (C_{ob})	3.5pF	6pF	–
Input Capacitance (C_{ib})	9pF	–	–
Turn-on time (t_{on})	35ns	35ns	35ns
Turn-off time (t_{off})	300ns	300ns	285ns

3.1 No-Load Test of the Proposed RGD

For the no-load test, the DC power supply (TT-Technic MCH303DII) which outputs +12 V is used to supply the transistors. To display and analyze the output waveform, the GWinstek GDS2202A oscilloscope is used in real time-tests. Also, the GWinstek SFG1003 function generator is utilized to generate the PWM signal. In this experimental study, the proposed gate driver circuit designed for the power

MOSFETs located on boost converters is compared with the driver circuits introduced in [4] and [39], and the IR2121 integrated circuit. In the no-load test, the frequency of the PWM signal is adjusted to 1 MHz. The function generator has the capability to generate the signal up to 88% duty cycle. For this reason, the maximum 88% duty cycle is handled in the experimental analysis mentioned in this subsection. In addition, the oscilloscope has two ports. Therefore, only the waveforms of the input and output signals are given. Note that in real-time applications, the values may differ due to the non-ideal parameters of the components and the devices. Note that all figures are obtained by the oscilloscope.

In the no load test, the frequency and the duty cycle are set as 1 MHz and 0.9, respectively. Figures 6a and 6b show the input and output waveforms of the proposed driver and IR2121 to analyze the fall edges. It can be seen from Figure 6a that the time delay between the fall edges of the input and output signals is 30 ns, for the proposed driver. Also, the duty cycle of the output signal is 0.8628, while the input duty cycle is 0.8780 which is the maximum range at 1 MHz. On the other side, from Figure 6b, time delay between the fall edges of the input and output signals is measured as 348 ns for IR2121. Moreover, the duty cycle of the output signal is 0.8979, while the input duty cycle is 0.7697. The point to be noted here is that when the input duty cycle increases, no PWM signal is observed at the output.

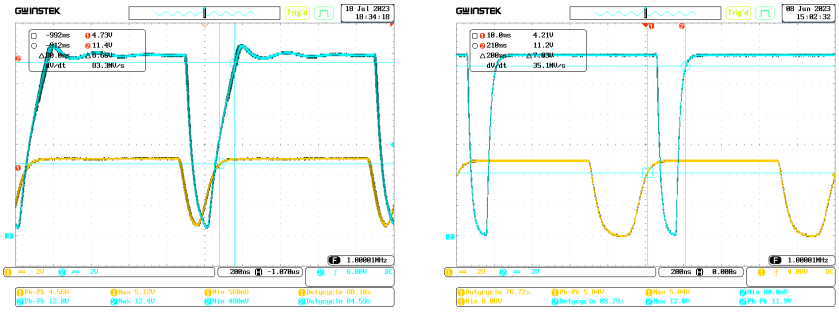


(a) (b)

Figure 6

The waveforms for the analysis of the fall edges of the input and output signals: (a) the waveforms of input and output signals of the proposed RGD, (b) the waveforms of input and output signals of IR2121. The yellow line represents the input signal, and the blue line represents the output signal.

From Figure 7a, the time delay between the rise edges of the input and output signals of the proposed driver is 80 ns. On the contrary, from Figure 7b, the time delay between the rise edges of the input and output signals of the IR2121 is 200 ns.



(a) (b)

Figure 7

The waveforms for the analysis of the rise edges of the input and output signals: (a) the waveforms of input and output signals of the proposed RGD, (b) the waveforms of input and output signals of IR2121. The yellow line represents the input signal, and the blue line represents the output signal.

Table 4

Comparison of the proposed RGD with other proposed gate drive circuits and commercially-availabla IC-based gate driver

Parameters	**Proposed Gate Driver**	**IR2121**	**Gate Driver in [4]**	**Gate Driver in [39]**
Rise/Fall Time of Edges (ns)	140	95	180	55
Switching Frequency (MHz)	$0-1$	$0-1$	$0-1$	0.5
Max. Power Consumption (mW)	120	72	1193	500
Duty Cycle Range (%)	$12-90$	$12-90$	$15-90$	$10-90$
Cost ($)	<5	<5	N/A	~170
Drive Voltage (V)	$0/+12$	$0/+12$	$-5/+15$	$0/+25$

For comparisons, some parameters such as rise/fall time of edges, switching frequency, power consumption, duty ratio, cost and drive voltage are given in Table 4. The fall/rise times are less than the driver circuit presented in [39] and the IR2121 driver, even the total time delay between input and output is about 160 ns and is lower than these circuits. Moreover, the proposed driver circuit has reached a switching frequency of 1 MHz. In the context of power consumption, it consumes less power than the circuits introduced in [4] and [39]. However, it consumes more power than the IR2121 driver due to the passive components. The proposed driver has the lowest cost in terms of cost comparison. Although the sum of the on-off times calculated by Eq. 22 and Eq. 25 is higher than the on-off times of IR2121, the delays between the rising edges and the falling edges are less than IR2121 due to the shutdown propagation delay of IR2121. It can be clearly seen from Figure 6 and Figure 7. This delay causes a less sensitive duty ratio adjusting for IR2121.

3.2 The Load Test of the Proposed RGD

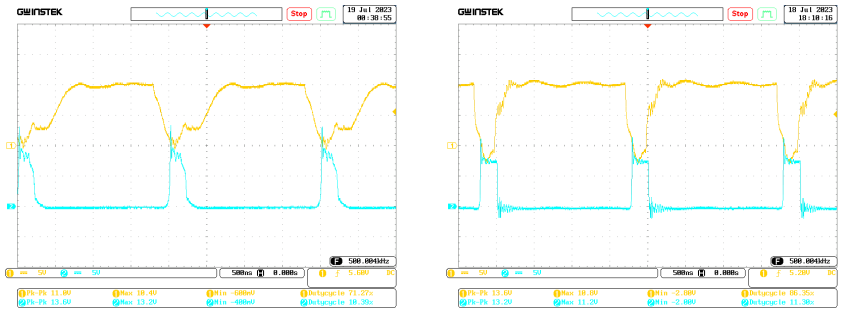
In this subsection, the proposed RGD is tested under the load. The experimental test platform as shown in Figure 4 is set up with the data given in Table 5. The proposed driver is tested at 500 kHz due to the limitations of the converter, with duty cycle rates of 0.12 and 0.90, respectively. The IRFP460 power MOSFET placed in the DC-DC converter is selected for experimental analysis to test the proposed RGD.

Table 5
Some parameters of experimental platform

Parameters	**Proposed Gate Driver**
Drive Voltage	12 V
Switching Frequency	0.5 MHz
Output Voltage of DC-DC Converter ($V_{maximum}$)	500 V
MOSFET in DC-DC Converter	IRFP460 n
Load Resistance	100 W 1 kΩ
The Inductor Placed in DC-DC Converter	34 µH
Load Capacitance	1500 µF

Note that all figures are obtained by the oscilloscope and since the oscilloscope has two probes, the output signal of the proposed gate driver is demonstrated with the output signal of the microcontroller which is applied to the gate drive circuit as the input, also in another demonstration, the output of the boost converter can be measured with the output signal and represented together. Furthermore, the display of the V_{DS} is observed by setting the probe to 10X. Figure 8a shows the output signal of the proposed RGD, which is simultaneously the V_{GS} signal. The duty cycle ratio of the input PWM signal is applied as 0.892 due to the limits of the function generator. The proposed gate driver generated a duty cycle of 71.27%. The duty cycle between the Drain-Source terminals is 10.39%. The peak voltage between the Drain-Source terminals of the MOSFET is observed to be a maximum of 132 V. V_{GS} is approximately 3 V at the resonant stage and 10.4 V at the clamping stage. There is practically no oscillation during the turn-off stage. The negative voltage sag of V_{GS} is observed as -0.60 V. In contrast to the proposed RGD, as shown in Figure 8b, IR2121 generated a duty cycle of 86.35%. Also, the duty cycle between the Drain-Source terminals is 11.30%, the peak voltage between the Drain-Source terminals is observed as 112 V and the negative voltage sag of V_{GS} is observed as -2.80 V. However, high-frequency oscillations are superimposed on V_{GS} during the turn-on stage. This situation also creates high-frequency oscillations during the turn-off of V_{DS} and so, the negative voltage sag of V_{DS} is -20 V. Figure 9a demonstrates V_{GS} and V_{DS} of the proposed RGD with a duty cycle rate of 11.02%. The output duty cycle is observed as 19.13%. The peak value of V_{GS} is observed as 3.68 V. As seen in Figure 9a, for V_{GS}, the negative voltage spike of -1.84 V is observed with an oscillation of about 2 MHZ. On the other side, the duty cycle ratio for V_{DS} is 87.04%. Accordingly, the maximum and the minimum values of the V_{DS}

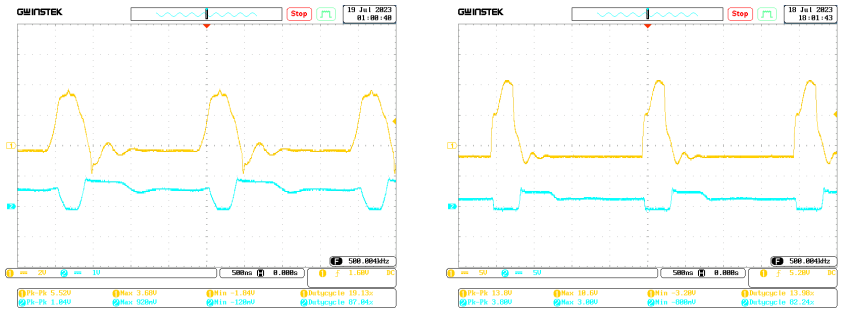
are 9.20 V and −1.20 V, respectively. In contrast to the proposed RGD, as clear in Figure 9b, IR2121 generated a duty cycle of 13.98%. The peak of V_{GS} is 10.60 V. It can be seen that the negative voltage sag of −3.2 V is observed with an oscillation of about 2 MHZ. Furthermore, the duty cycle ratio of V_{DS} is 82.24%. The maximum and the minimum values of V_{DS} are 30 V and −8 V, respectively.



(a) (b)

Figure 8

The waveforms of V_{GS} and V_{DS} for load test with approximately %90 input duty cycle: (a) the waveforms obtained by the proposed RGD, (b) the waveforms obtained by IR2121. The yellow line represents V_{GS}, and the blue line represents V_{DS}.



(a) (b)

Figure 9

The waveforms of V_{GS} and V_{DS} for load test with approximately %10 input duty cycle: (a) the waveforms obtained by the proposed RGD, (b) the waveforms obtained by IR2121. The yellow line represents V_{GS}, and the blue line represents V_{DS}.

The delay time of RGD is about 230 ns, regardless of the frequency. For performance and applicability, the data of the RGD proposed in Table 6 and Table 7 are compared with the drivers proposed in [4] and [39] and with IR2121. The total power consumption of the driver is less than 1W during the duty cycle ranging from 0.1 to 0.9. The input capacity of the MOSFET in the DC-DC converter is very high, which increases the Miller effect and limits the duty cycle rate. This case is clear

from Figure 8a. Although the resonance decreased on VDS, the duty cycle is observed as approximately 72% and VGS is about 4V at the resonant stage of turn-on. These values are caused by the hard characteristics of the MOSFET in DC-DC converter. It can be observed from Figure 8 that the proposed RGD has reduced the transient oscillations on MOSFET. As can be seen from Tables 6 and 7, the proposed RGD has low power losses. Unlike the resonant transformer, which limits the high switching capability, the proposed RGD can be capable of achieving high frequencies thanks to the air core inductor. Also, it may drive SiC components over 1 MHz.

Table 6
Comparison of proposed RGD with the input duty cycle of 90%

Parameters	**Proposed Gate Driver**	**IR2121**	**Gate Driver in [4]**	**Gate Driver in [39]**
Switching Frequency (MHz)	0.5	0.5	0.5	0.2
Max. Power Consumption (mW)	< 100	< 100	1473	1100
Output Duty Cycle (%)	~ 72	~ 86	90	NA
Maximum V_{GS} (V)	10.4	10.8	18	NA
Minimum V_{GS} (V)	-0.60	-2.80	< -5	NA

Table 7
Comparison of proposed RGD with the input duty cycle of 10%

Parameters	**Proposed Gate Driver**	**IR2121**	**Gate Driver in [4]**	**Gate Driver in [39]**
Switching Frequency (MHz)	0.5	0.5	0.5	0.2
Max. Power Consumption (mW)	529	178	1473	1100
Output Duty Cycle (%)	~ 19	~ 14	15	NA
Maximum V_{GS} (V)	10.4	10.8	18	NA
Minimum V_{GS} (V)	-1.84	-3.20	< -5	NA

Table 8
Comparison of proposed RGD with other gate drivers

Parameters	**Ref [4]**	**Ref [16]**	**Ref [22]**	**Ref [28]**	**Ref [39]**	**Ref [44]**	**Proposed RGD**
Number of Switches	8	4	2	2	8	4	4
Number of Diodes	1	1	2	3	–	–	–
Transformers	1	–	–	–	1	–	–
Gate Voltage	15V	20V	20V	20V	25V	15V	12V
Test Bench Current	73A	150A	10A	12A	212A	70A	20A
Test Bench Voltage	900V	550V	800V	500V	600V	500V	500V
Conduction Loss	HIGH	LOW	LOW	LOW	LOW	LOW	LOW
Test Bench frequency (kHz)	500	–	70	400	500	500	500

Furthermore, the proposed RGD is compared with similar gate drivers which exist in the literature in terms of structure, capability, and test bench. Comparison results are listed in Table 8. As can be seen in Table 8, for all schemes include four or more semiconductor elements such as diodes and switches. The proposed RGD contains four semiconductor elements. These results show that the proposed RGD has low conduction losses as much as other drivers proposed in the literature.

Conclusions

The RGD with an adjustable duty ratio, for discrete devices, such as the power MOSFET, SiC MOSFET and IGBT, is proposed in this study to achieve the wide ratio of duty cycle with low power consumption. It is suitable for high-speed switching thanks to the MOSFET connected to the input of driver. Due to the high-gain and easy-to-control BJT, the voltage is shifted to 12 V. The resonance inductor has virtually eliminated high frequency oscillations on the power MOSFET. This is an effective approach for VGS raising and falling edges without high-frequency oscillations. The proposed RDD is achieved the duty cycle between 0.19 to 0.72, when using power MOSFET at 500 kHz. Also, the total power losses are less than 100mW. In terms of cost evaluation, due to its non-complex structure and the low cost of the components used, the total cost is less than $5 (USD).

In terms of performance criteria, in comparison to gate drives in literature, the proposed RGD has an equal switching frequency, lower cost, and lower power consumption. However, the proposed circuit has several disadvantages. First, it takes up more space in PCBs. Also, it is not suitable for use at frequencies over approximately 4 MHz. Besides these disadvantages, using the proposed gate drive circuit, with a microcontroller-based application, provides the capability for flexible control in grid-connected PV-home systems and can make it useful for similar areas, such as plug-in electric vehicles and energy storage systems.

In the tests under load, at switching frequencies up to 500 kHz, no out-of-bound thermal losses are observed, in the switching elements. This is proof that the proposed gate driver circuit has a high performance and robust design. This is achieved despite the use of circuit elements with high thermal resistance values in the design of the proposed driver circuit, and no thermal stress occurs even under loaded conditions, on the circuit and on the MOSFET, in DC-DC converter. This shows that the thermal losses can be kept at a low level, even when operating at very high switching frequencies, as a result of hardware improvements to be made on the proposed gate driver circuit. In addition, the proposed driver circuit will constitute an alternative, avoiding the difficulties encountered in the low supply of the embedded circuit technologies, available in today's scarce conditions.

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